

REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Non-Final Office Action dated February 19, 2003 has been received and its contents carefully noted. Claims 1-11 and 13 have been amended to better conform to U.S. practice and we believe they have not been narrowed for he patentability reason. Claims 14-18 are newly added. Accordingly, claims 1-18 are pending in this application.

In the Office Action, claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,997,940 issued to Akiyama et al. ("Akiyama"). Applicants respectfully traverse these rejections and reconsideration is hereby requested.

Claims 1-2 were objected as containing informalities. Applicants address each of these objections in detail below.

Applicants wish to thank the Examiner for objecting to claims 2-13 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. As to claims 5-13, Applicants understand that these claims are currently allowable.

Claim Objections

Claims 1-2 were objected to because of minor informalities. Applicants, respectfully submit that amended claims 1-2 and 13 are in full compliance with the Examiner's objections and respectfully request withdrawal of the objections.

Rejections Under 35 U.S.C. § 103

In the Office Action, claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Akiyama. Applicants respectfully traverse this rejection and reconsideration is hereby requested.

Claim 1 is allowable as it recites a combination of elements, including, “a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.” None of the cited references singly or in combination teaches or suggests at least these features. Accordingly, Applicants respectfully submit that independent claim 1 and dependent claims 2-3 are in condition for allowance.

Other Matters

Newly added claims 14-18 are allowable over the cited references. Claims 14-15 depend on allowable claim 7. Newly added claims 16-18 require a combination of elements including, for example, “a level shift unit in electrical communication with the second control signal for generating an inverting signal.” None of the cited references singly or in combination teaches or suggests at least these features. Accordingly, Applicants respectfully submit that independent claim 16 and dependent claim 18 are in condition for allowance.

CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn.

Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 1-18 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

It is not believed that any extensions of time or fees for net addition of claims are required at this moment. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 23-1951. Please credit any overpayment to deposit Account No. 23-1951.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,


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APPENDIX

The “marked-up” version of the amended claim is as follows:

1. (Amended) A liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for [outputting] selectively providing the image signals to a third electrode from a first electrode connected to the source signal line [or stopping the same] depending on voltage state of a second electrode connected to the scan signal line;

a power unit for respectively supplying first power and second power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit [respectively] including a first control signal line for transmitting a first control signal to all pixels from outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from the outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting [or blocking light] according to voltage difference between the image signals and the second power; and

a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.[,]

2. (Amended) The liquid crystal display (LCD) of claim 1, wherein an operation mode image signal output by the third electrode of the pixel switch is transmitted to the liquid crystal unit, when the first control signal is in low state and the second control signal is in high state, and when the first control signal is in high state[, either a still mode image signal output by the third

electrode of the pixel switch or its inverting signal is transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states according to characteristics of the LCD panel].

3. (Amended) The liquid crystal display (LCD) of claim 1, wherein the memory cell unit further comprises:

a first inverter circuit [having] including a[n] nTFT and a pTFT, a drain electrode of the nTFT [being] is connected to [that of] the pTFT, and gate electrodes of the first inverter circuit are [being] connected to the third electrode of the pixel switch;

a second inverter circuit [having] including a[n] nTFT and a pTFT, drain electrodes of the [nTFT and pTFT] second inverter circuit [being] are connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit [being] are connected to the drain electrodes of the first inverter circuit;

a push nTFT [having] including a drain electrode connected to the first power, a source electrode [is] connected to a source [electrodes] electrode of the pTFTs of the first and second inverter [circuit] circuits [and the second inverter circuit,] and a gate electrode of the push nTFT [is] connected to the first control signal line;

a pull nTFT [having] including a source electrode connected to the second power, a drain electrode [is] connected to source electrodes of the nTFTs of the first and second inverter circuit [and the second inverter circuit,] and a gate electrode of the pull nTFT [is] connected to the first control signal line;

an operation nTFT [having] including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT are connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still pTFT [having] including a gate electrode connected to the second control signal line, and source and drain electrodes of the still pTFT [are] connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

4. (Amended) The liquid crystal display (LCD) of claim 1, wherein the control signal line unit transmits [respective] control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions [either in horizontal direction or, in vertical direction].

5. (Amended) A low power liquid crystal display (LCD), comprising:

- a scan signal line for supplying scanning signals to pixels configuring an LCD panel;
- a source signal line for supplying image signals to pixels configuring the LCD panel;
- a pixel switch for [outputting]selectively outputting the image signals to a third electrode from a first electrode connected to the source signal line [or stopping the same] depending on voltage state of a second electrode connected to the scan signal line;
- a power unit for [respectively] supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel;
- a control signal line unit [respectively] including a first control signal line for transmitting a first control signal to all pixels from the outside of the pixel area of the LCD

panel, and a second control signal line for transmitting a second control signal to all pixels from outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting [or blocking light] according to a difference between the image signals and the third power; and

a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting signal.

6. (Amended) The liquid crystal display (LCD) of claim 5, further comprising a memory cell unit.

7. (Amended) The liquid crystal display (LCD) of claim 6, wherein the memory cell unit receives the first and second control signals from the control signal line unit and receiving the inverting signal of the second control signal output by the level shift unit[.].

8. (Amended) The liquid crystal display of (LCD) claim 7, wherein[, when the first control signal is in low state and the second control signal is in high state,]an operation mode image signal is selectively output by a third electrode of the pixel switch and the operation mode signal is selectively transmitted to the liquid crystal unit[, and when the first control signal is in high state, either a still mode image signal output by the third electrode of the pixel switch or its inverting signal is transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states according to characteristics of the LCD panel].

9. (Amended) The liquid crystal display (LCD) of claim 7, wherein the memory cell unit comprises:

a first inverter circuit [having] including a[n] nTFT and a pTFT, a drain electrode of the nTFT [being] [is] connected to [that of] the pTFT, and gate electrodes of the first inverter circuit [nTFT and pTFT] [being] are connected to the third electrode of the pixel switch;

a second inverter circuit [having] including a[n] nTFT and a pTFT, drain electrodes of the nTFT and pTFT [being] [are] connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit nTFT and pTFT [being] are connected to the drain electrodes of the first inverter circuit;

a push nTFT [having] including a drain electrode connected to the first power, a source electrode connected to source electrodes of the pTFTs of the first and second inverter [circuit] circuits [and the second inverter circuit], and a gate electrode connected to the first control signal line;

a pull nTFT [having] including a source electrode connected to the third power, a drain electrode connected to source electrodes of the nTFTs of the first and second inverter [circuit] circuits and the second inverter circuit, and a gate electrode connected to the first control signal line;

an operation nTFT [having] including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT [are] connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still nTFT [having] including a gate electrode connected to receive an inverting signal of the second control signal output by the level shift unit, and source and drain electrodes of the

still nTFT [are] connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

10. (Amended) The liquid crystal display (LCD) of claim 5, wherein the level shift unit comprises:

a third inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT [being] is connected to that of the pTFT of the third inverter circuit, gate electrodes [being] are connected to the second control signal line, a source electrode of the pTFT [being] is connected to the second power, and a source electrode of the nTFT [being] is connected to the third power; and

a level-up pTFT having a gate electrode connected to a drain electrode of the third inverter circuit, a source electrode of the level-up pTFT is connected to the second power, and a drain electrode of the level-up pTFT is connected to the second control signal line.

11. (Amended) The liquid crystal display (LCD) of claim 5, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions[either in horizontal direction or in vertical direction].

12. (Not Amended) In a liquid crystal display (LCD) panel driving method for a pixel switch that receives scanning signals and image signals from scanning signal lines and source signal lines to output the image signals to a memory cell unit that is operated by first and second

control signals or stops the image signals to display the same, an LCD driving method comprising:

the memory cell unit transmitting operation mode image signals output by the pixel switch to liquid crystal and displaying the same when the first control signal is in low state and the second control signal is in high state; and

transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state.

13. (Amended) The method of claim [8]12, wherein the method further comprises transmitting respective control signals sequentially delayed by a buffer circuit to a corresponding pixel area when the pixel area of the LCD panel is divided into at least two portions in either a horizontal or vertical direction.

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